Amendments to the Specification

Please replace the title with the following amended title:

A DICED SEMICONDUCTOR DEVICE HAVING NARROW KERF AREA ~~AND METHOD OF MANUFACTURING THE SAME~~

Please replace the paragraph beginning on page 2, line 14 with the following amended paragraph:

However, when the above-mentioned dicing method using the blade is utilized, there is a need to set a margin ranging from several tens of μm to several hundreds of μm rather than a chip size. This is because a [[curf]] kerf width produced upon dicing, pitching developed by impact of dicing, etc. must be taken into consideration.

Please replace the paragraph beginning on page 2, line 21 with the following amended paragraph:

When the SOS substrate is used in particular, a long period of time is required for dicing because the sapphire substrate is a grinding resistant material, and this is another issue to consider in addition to ~~the occurrence of the curf~~ kerf width and dicing. As a result, the blade is wasted earlier, thus causing a substantial increase in cost.

Please replace the paragraph beginning on page 2, line 27 with the following amended paragraph:

On the other hand, when the above non-heated processing system (or also called non-fusion system) is utilized, the [[curf]] kerf width and pitching are almost undeveloped and high-speed dicing is made possible as compared with the dicing method using the blade.

Please replace the paragraph beginning on page 3, line 9 with the following amended paragraph:

At this time, the rate of convergence of the laser light into the target is reduced due to the fact that the execution of dicing becomes impossible or the laser light is scattered over the surface of the target. As a result, a remarkable [[curf]] kerf width and pitching might be developed.

Please replace the paragraph beginning on page 3, line 16 with the following amended paragraph:

With an increase in demand for high integration of a recent semiconductor device, the practical application of a thinned silicon substrate or the like is urgently necessary. Since, however, the [[curf]] kerf width and pitching become noticeable with substrate's thinning, many technical problems ~~arises~~ arise under existing circumstances.

Please replace the paragraph beginning on page 3, line 20 with the following amended paragraph:

Therefore, an object of the present invention is to provide a semiconductor device which makes it possible to apply non-fusion type dicing using laser light regardless of a structural form of a target to be processed, thereby to suppress the occurrence of a [[curf]] kerf width and pitching, and a manufacturing method thereof.

Please replace the paragraph beginning on page 6, line 22 with the following amended paragraph:

~~Fig. 1~~ Fig. 1(A) is a schematic plan view showing part of a wafer prior to being diced into semiconductor devices [[each]] and Fig. 1(B) illustrates a configuration of a light irradiation device in relation to a target, according to a first embodiment of the present invention.

Please replace the paragraph beginning on page 7, line 10 with the following amended paragraph:

Figs. 6(A) through [[6(D)]] 6(C) are process diagrams (part 1) for describing a process for manufacturing the semiconductor device according to the fourth embodiment of the present invention.

Please replace the paragraph beginning on page 7, line 16 with the following amended paragraph:

Figs. 8(A) through [[8(D)]] 8(C) are process diagrams for describing a process for manufacturing a semiconductor device according to a fifth embodiment of the present invention.

Please replace the paragraph beginning on page 7, line 21 with the following amended paragraph:

Embodiments of the present invention will hereinafter be explained with reference to Figs. 1(A) through 8(C) ~~Figs. 1 through 8~~. Incidentally, the respective drawings schematically show [[one]] configurational examples of semiconductor devices according to the present invention. Also the respective drawings simply schematically illustrate shapes, sizes of respective components and their layout relationships to the extent of making it possible to understand the present invention. The present invention is by no means limited to these illustrated examples. In order to make it easy to understand the drawings, hatchings (i.e., oblique lines) indicative of cross-sections are omitted except for parts. Although particular materials and conditions or the like might be used in the following description, these materials and conditions are nothing but one preferred example. Accordingly, [[any]] no limitations are imposed on them. Similar components illustrated in the respective drawings are respectively identified by the same reference numerals, and the description of certain common components might be

omitted.

Please replace the paragraph beginning on page 8, line 10 with the following amended paragraph:

A semiconductor device according to a first embodiment of the present invention and its manufacturing method will be explained with reference to Figs. 1(A) through 2(D). Fig. 1(A) ~~Figs. 1 and 2. Fig. 1~~ is a plan view schematically showing part of a wafer prior to being diced into the semiconductor devices [[each]] according to the present embodiment. Fig. 2(A) is a cross-sectional view as seen in the direction indicated by arrows in the drawing, of a cut area (i.e., a cross-section) obtained by cutting ~~Fig. 1~~ Fig. 1(A) along an alternate long and short dash line A - A. Figs. 2(B) through 2(D) are cross-sectional views following Fig. 2(A), for describing the semiconductor devices each according to the present embodiment and the manufacturing method thereof.

Please replace the paragraph beginning on page 14, line 5 with the following amended paragraph:

Therefore, the occurrence of a [[curf]] kerf width and pitching can be suppressed as compared with the case in which the individualization into the chips is done by only the dicing method using the blade as before.

Please replace the paragraph beginning on page 14, line 14 with the following amended paragraph:

A second embodiment of the present invention will be explained with reference to ~~Fig. 3~~[[.]] Figs. 3(A) through 3(D), which are respectively cross-sectional views similar to Figs. 2(A) through 2(D), for describing a semiconductor device according to the present embodiment and its manufacturing method. Incidentally, the same elements of structure as those already described in the first embodiment are respectively identified by the same reference numerals, and their specific description will be omitted (the following embodiments are also similar).

Please replace the paragraph beginning on page 16, line 25 with the following amended paragraph:

Therefore, the occurrence of a [[curf]] kerf width and pitching noticeable with respect to the thinned silicon substrate or the like can be suppressed in the dicing process.

Please replace the paragraph beginning on page 17, line 5 with the following amended paragraph:

A third embodiment of the present invention will be explained with reference to ~~Fig. 4~~[[.]] Figs. 4(A) through 4(D), which are respectively cross-sectional views similar to Figs. 2(A) through 2(D), for describing a semiconductor device according to the present

embodiment and its manufacturing method.

Please replace the paragraph beginning on page 18, line 21 with the following amended paragraph:

A semiconductor device according to a fourth embodiment of the present invention and its manufacturing method will be explained with reference to Figs. 5 through [[7]] 7(B). Fig. 5 is a plan view schematically showing part of a wafer prior to [[be]] being diced into the semiconductor devices each according to the present embodiment. Fig. 6(A) is a cross-sectional view as seen in the direction indicated by arrows in the drawing, of a cut area (i.e., cross-section) obtained by cutting Fig. 5 along an alternate long and short dash line B-B. Figs. 6(B) through 7(B) are respectively cross-sectional views following Fig. 6(A) for describing the semiconductor devices each according to the present embodiment and the manufacturing method thereof. The present embodiment will explain WCSP as one example with a target to be processed requiring a dicing process as a structure having a seal layer.

Please replace the paragraph beginning on page 21, line 13 with the following amended paragraph:

Thus, modified portions 23 are formed inside the silicon substrate 42 by the laser light gathered with high accuracy, in a manner similar to the first embodiment. Then the silicon substrate 42 portion can be cut using cracks 68 with the modified portions 23 as

starting points. Thus, a laminated body 651 including the cracks 68 and dicing residual areas [[60a]] 62a (see Fig. 7(A)) formed in the silicon substrate 42 is obtained on the dicing tape 66 along the dicing area 62. Incidentally, since the electrode pads 46b and seal layers 55b are respectively the permeability resistant portions, the second layers 47 remain in the dicing area 62 with the cutting thereof after the completion of the dicing process.

Please replace the paragraph beginning on page 23, line 10 with the following amended paragraph:

Therefore, the occurrence of a [[curf]] kerf width and pitching noticeable with respect to the thinned silicon substrate or the like can be suppressed in the dicing process.

Please replace the paragraph beginning on page 23, line 17 with the following amended paragraph:

A semiconductor device according to a fifth embodiment of the present invention and its manufacturing method will be explained with reference to ~~Fig. 8~~[[.]] Figs. 8(A) through [[8(D)]] 8(C), which are respectively cross-sectional views similar to Figs. 2(A) through 2(D), for describing the semiconductor device according to the present embodiment and its manufacturing method.

Please replace the paragraph beginning on page 24, line 6 with the following amended paragraph:

Thereafter, as shown in Fig. 8(A), the back surface f of the silicon substrate 42 of the laminated body 65 as described in the fourth embodiment is first fixed onto a dicing tape [[74]] 66.

Please replace the paragraph beginning on page 24, line 27 with the following amended paragraph:

Thereafter, a peeling process for peeling away the respective cut WCSPs 100 from the dicing tape [[70]] 66 is performed in a manner similar to the fourth embodiment (see Fig. 7(B)).

Please replace the paragraph beginning on page 27, line 4 with the following amended paragraph:

As a result, the occurrence of a [[curf]] kerf width and pitching can be suppressed as compared with a dicing method using a blade as before, thus making it possible to realize a size reduction in semiconductor device.